CLAIMS

1.

An integrated circuit structure for MOS-type devices comprising:

a silicon substrate (3) of a first conductivity type;

first gate insulating regions (2) selectively placed over the silicon substrate (3) of the first conductivity type;

a first polycrystalline silicon layer (6) selectively placed over the silicon substrate (3) of the first conductivity type;

second gate insulating regions (7) selectively placed over the first gate insulating regions (2) and the first polycrystalline silicon layer (6);

a second polycrystalline silicon layer (8) selectively placed over the second gate insulating regions (7);

first buried silicon regions (5) of a second conductivity type, buried within the silicon substrate (3) of the first conductivity type, placed under the first polycrystalline silicon layer (6) and in contact therewith; and

second buried silicon regions (15) of the second conductivity type, buried within the silicon substrate (3) of the first conductivity type, placed under the second gate insulating regions (7), under the second polycrystalline silicon layer (8) and insulated therefrom.

2.

The integrated circuit structure of claim 1, further comprising third buried silicon regions (9) of the second conductivity type, buried within the silicon substrate (3) of the first conductivity type, placed under the first gate insulating regions (2) and the second gate insulating regions (7), and being insulated from the first polycrystalline silicon layer (6) and the second polycrystalline silicon layer (8).

3.

The integrated circuit structure of claim 1, further comprising:

a silicon substrate of the second conductivity type, buried within the silicon

substrate (3) of the first conductivity type; and

first and second buried silicon regions of the first conductivity type, buried within the silicon substrate of the second conductivity type,

wherein

said first gate insulating regions (2) are selectively placed over the silicon substrate of the second conductivity type;

said first polycrystalline silicon layer (6) is selectively placed over the silicon substrate of the second conductivity type;

said first buried silicon regions of the first conductivity type are placed under the first polycrystalline silicon layer (6) and in contact therewith; and

said second buried silicon regions of the first conductivity type are placed under the second gate insulating regions (7), under the second polycrystalline silicon layer (8) and insulated therefrom.

4.

The integrated circuit structure of claim 3, further comprising third buried silicon regions of the first conductivity type, buried within the silicon substrate of the second conductivity type, placed under the first gate insulating regions (2) and the second gate insulating regions (7), and being insulated from the first polycrystalline silicon layer (6) and the second polycrystalline silicon layer (8).

5.

A process for forming an integrated circuit structure, comprising the steps of:

providing a silicon substrate (3) of a first conductivity type;

depositing a first insulating layer over the silicon substrate of the first conductivity type;

forming first gate insulating regions (2) in the insulating layer;

forming first and second buried silicon regions (5, 15) of a second conductivity type within the silicon substrate of the first conductivity type;

depositing a first polycrystalline silicon layer (6), said first polycrystalline silicon layer contacting said first buried silicon regions (5);

depositing a second insulating layer over the first insulating layer, the first polycrystalline silicon layer and the second buried silicon regions (15); and

depositing a second polycrystalline silicon layer over said second insulating layer and said second buried silicon regions (15) of the second conductivity type, said second buried silicon regions of the second conductivity type being insulated from said second polycrystalline silicon layer.

6.

The process of claim 5, further providing the step of forming third buried silicon regions (9) of the second conductivity type within the silicon substrate of the first conductivity type.

7.

The process of claim 5, further providing the steps of:

providing a silicon substrate of the second conductivity type, buried within the silicon substrate of the first conductivity type;

forming first and second buried silicon regions of the first conductivity type, buried within the silicon substrate of the second conductivity type,

wherein

said first gate insulating regions (2) are selectively placed over the silicon substrate of the second conductivity type;

said first polycrystalline silicon layer (6) is selectively placed over the silicon substrate of the second conductivity type;

said first buried silicon regions of the first conductivity type are placed under the first polycrystalline silicon layer (6) and

said second buried silicon regions of the first conductivity type are placed under the second gate insulating regions (7) and the second polycrystalline silicon layer (8).

8.

The process of claim 7, further providing the step of forming third buried silicon regions of the first conductivity type, buried within the silicon substrate of the second

conductivity type, placed under the first gate insulating regions (2) and the second gate insulating regions (7), and being insulated from the first polycrystalline silicon layer (6) and the second polycrystalline silicon layer (8).

9.

In an integrated circuit structure for MOS-type devices comprising a silicon substrate (3) of a first conductivity type, a first-level polysilicon layer (6), a second-level polysilicon layer (8) and buried silicon regions (5, 9, 15) of a second conductivity type buried within the silicon substrate (3) of the first conductivity type,

the improvement comprising an arrangement for programmably connecting the buried silicon regions of the second conductivity type to the polysilicon layers or alternatively programmably isolating the buried silicon regions of the second conductivity type from the polysilicon layers.

10.

The arrangement of claim 9,

wherein programmably connected buried silicon regions of the second conductivity type (5) are connected to the first-level polysilicon layer (6).

11.

The arrangement of claim 9, wherein the integrated circuit structure further comprises:

a silicon substrate of the second conductivity type, buried within the silicon substrate (3) of the first conductivity type; and

buried silicon regions of the first conductivity type buried within the silicon substrate of the second conductivity type,

and wherein an arrangement for programmably connecting the buried silicon regions of the first conductivity type to the polysilicon layers or alternatively isolating the buried silicon regions of the first conductivity type from the polysilicon layers is further comprised.

12.

The arrangement of claim 11,
wherein programmably connected buried silicon regions of the first conductivity type are connected to the first-level polysilicon layer.

13.

A process for forming a programmable multi-level polysilicon device in an integrated MOS-type circuit structure, comprising the steps of:

providing a silicon substrate (3) of a first conductivity type;

forming buried silicon regions (5, 9, 15) of a second conductivity type within the silicon substrate (3) of the first conductivity type;

depositing a first polycrystalline silicon layer over the silicon substrate (3) of the first conductivity type; and

depositing a second polycrystalline silicon layer over the silicon substrate (3) of the first conductivity type,

wherein a first portion (5) of said buried silicon regions of the second conductivity type contacts the first polycrystalline silicon layer and is isolated from the second polycrystalline silicon layer, and a second portion (15) of said buried silicon regions is insulated from the first and the second polycrystalline silicon layer.

14.

The process of claim 13, further comprising the steps of:

providing a silicon substrate of a second conductivity type, buried within the silicon substrate (3) of the first conductivity type;

forming buried silicon regions of the first conductivity type within the silicon substrate of the second conductivity type;

depositing the first polycrystalline silicon layer over the silicon substrate of the second conductivity type; and

depositing the second polycrystalline silicon layer over the silicon substrate of the second conductivity type,

wherein a first portion of said buried silicon regions of the first conductivity type contacts the first polycrystalline silicon layer, and a second portion of said buried silicon

regions of the second conductivity type is insulated from the first and second polycrystalline silicon layer.